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EXAMINER
VIGUSHIN, JOHN B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,100	FRITZ, DONALD S.	
	Examiner	Art Unit	
	John B. Vigushin	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *31 and 32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-30, drawn to a semiconductor package, classified in class 257, subclass 778.

II. Claims 31-32, drawn to method of underfilling a gap in the semiconductor package, classified in class 438, subclass 126.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process not requiring the step of forming a channel.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Attorney Francis E. Morris on February 28, 2003, a provisional election was made with traverse to prosecute the invention of Group I, Claims 1-30. Affirmation of this election must be made by applicant in replying to this Office action. Claims 31-32 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Drawings

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the array of solder connections on the substrate wherein the number of solder connections in **one row** is less than the number of solder connections **in each of the remaining rows** of the solder connection array of the substrate **must be shown or the feature(s) canceled from Claims 29 and 30**. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

6. Claims 21, 22, 24 and 28 are objected to because of the following informalities:

In Claim 21, line 1: second occurrence of "further comprising" should be deleted.

In Claim 22, line 4: "allow" should be changed to --allowing--.

In Claim 24, line 3: "allow" should be changed to --allowing--.

In Claim 28, line 2: "under-fill" should be changed to --underfill--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112, 1st paragraph

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the

art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 1-16, 24-25, 29 and 30 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

In **Claim 1**, Applicant recites "a stress inhibiting intermediate mounting substrate" connected to "an interposer" and having a CTE smaller than "the interposer." The claimed structure indicates that the "stress inhibiting intermediate mounting substrate" is a distinct and separate structural element from the "interposer." However, there is **no support in the disclosure** for such a structure: The Specification and Drawings support a package structure wherein the "stress inhibiting intermediate mounting substrate" and the "interposer" **are one and the same structural element**; the descriptive terms "stress inhibiting intermediate mounting substrate" and "interposer" being used interchangeably to describe the identical structural element. The "interposer" as recited in lines 7 and 10 should be the "printed circuit board mounting substrate" supported in the disclosure. **Claim 2** should be cancelled and "interposer" in lines 7 and 10 of Claim 1 changed to --printed circuit board--, OR, perhaps, Claim 2 should be amended to change "interposer" to --stress inhibiting intermediate mounting substrate--.

Claims 2-16 depend from rejected base Claim 1 and therefore inherit the defects of the claim.

In **Claim 24**, Applicant recites "an interposer connected to said substrate through a second array of solder connections." Again, the "interposer" structure in lines 1 and 2 of Claim 24 has no support in the disclosure. The Specification and Drawings support the "substrate connected to said chip carrier through a first array of solder connections," as recited in line 3 of base Claim 22, as the **single contemplated interposer** of the invention: i.e., "said substrate" of **Claim 24 is** "the interposer" of the invention.

Claims 29 and 30 recite a structure wherein the array of solder connections of the substrate has a [single] row of solder connections wherein the number of solder connections in the row is less than the number of solder connections in each row of solder connections of the array of solder connections (Claim 29 recites "at least **one**" such additional row, and Claim 30 recites "a first row" having less solder connections than the other rows of the array). This structure is neither shown in Fig. 6 (wherein the top, bottom AND two middle rows interrupted by the access hole 650 have 16 solder connections, which is *less than* the other number of solder connections (18) in the other rows) nor discussed in the disclosure (p.9, lines 19-23 of Applicant's Specification only generally teaches removed or absent solder connections but does not disclose how the structure of Claims 29 and 30 is made or discuss the significance of **only one** row having less solder connections than the other rows of the array).

Claim Rejections - 35 USC § 112, 2nd paragraph

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 1-16 and 24-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites "an interposer" in lines 7 and 10. Since the disclosure only supports the "stress inhibiting intermediate mounting substrate" as the one and only one interposer of the invention, then in what sense is the recited "interposer" (lines 7 and 10) yet *another* functional "interposer" in the contemplated invention? It appears from the supporting disclosure that **Claim 2** should be cancelled and "interposer" in lines 7 and 10 of **Claim 1** should be changed to --printed circuit board mounting substrate--, OR, perhaps, Claim 2 should be amended to change "interposer" to --stress inhibiting intermediate mounting substrate--.

Claim 8 recites the limitation "said printed circuit board" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 14 recites the limitation "said solder bumps " in line 2. There is insufficient antecedent basis for this limitation in the claim. Furthermore, which solder "bumps" or "connections" are being referenced, the first array or the second array?

Claims 2-16 depend from rejected base Claim 1 and therefore inherit the defects of the claim.

Claim 24 (lines 1 and 2) and **Claim 25** (line 1) recite an "interposer." Since the disclosure only supports "said substrate" in line 2 of Claim 24 as the one and only one "interposer" of the invention, then in what sense is the recited "interposer" (lines 1 and 2) yet *another* functional "interposer" in the contemplated invention?

Rejections Based On Prior Art

11. The following references were relied upon for the rejections hereinbelow:

Alagaratnam et al. (US 6,335,491 B1)

Lyne (US 6,285,560 B1)

Beilin et al. (US 5,854,534)

Moore et al. (US 5,120,678)

Jackson et al. (US 6,333,563 B1)

Degani et al. (US 6,074,897)

Suzuki (US 5,650,918)

Kikuchi et al. (US 5,849,606)

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 22, 23 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Moore et al.

As to Claim 22, Moore et al. discloses, in Fig. 5: a chip carrier 102 to receive a semiconductor 100; a substrate 106 connected to carrier 102 through a first array of solder connections 98, substrate 106 adapted (with passage 122) for allowing access through the substrate 106 to one or more solder connections 98 (col.6: 22-54).

As to Claim 23, Moore et al. further discloses semiconductor 100 mounted to carrier 102 (Fig. 5; col.6: 30-32).

As to Claim 28, Moore et al. further discloses that access permits the insertion of underfill material (Fig. 5; col.6: 41-49).

14. Claim 30 is rejected under 35 U.S.C. 102(b) as being anticipated by Beilin et al.

Beilin et al. discloses a substrate 602B (Figs. 15, 17A,B and 18A,B) having a triangular array 602B (the bottommost triangular array in Fig. 17A, which, in conjunction with the other triangular arrays, is BGA solder-mounted to the next level of interconnect (col.15: 38-40) of solder connections 608B with a first (bottom) row of solder connections 608B (comprising only one connection) adjacent to a row of solder connections (the row above the first row comprising three connections) wherein the number of solder connections 608B in the first (bottom) row--i.e., only **one** connection--is less than the number of solder connections in each row of the solder connections above the first row in the triangular array 602B.

15. Claim 30 is rejected under 35 U.S.C. 102(b) as being anticipated by Kikuchi et al.

Kikuchi et al. (US 5,849,606) discloses a substrate 22 having a footprint matching the footprint 33 of BGA 34 of chip 11 (Figs. 14a and 14b; col.12: 60-65) and a first row of solder connections 32 (fourth row from the bottom row of chip 11 in Fig. 14a) adjacent to a row of solder connections 32 (the row of connections in the third of fifth row from the bottom row of chip 11 in Fig. 14a), wherein the number of solder connections 32 (five solder connections 32) in the first row (fourth row from the bottom row of chip 11 in Fig. 14a) is less than the number of solder connections 32 in each row of solder connections 32 of the BGA 34 (Fig. 14a).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 1-10, 13, 14 and 16 (as best understood by the Examiner in view of the 35 USC § 112, 2nd paragraph rejections above) and 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alagaratnam et al.

As to Claims 1 and 13:

I. Alagaratnam et al. discloses, in Figs. 2 and 3: a chip carrier 204; a semiconductor 206; chip carrier 204 having first coefficient of thermal expansion (CTE) different than the CTE of semiconductor 206 ($CTE_{semiconductor\ 206}$ = 2-4 PPM; $CTE_{carrier\ 204}$ = 6 PPM; col.2: 6-8; col.5: 51-53) and having semiconductor 206 mounted thereon (col.5: 5-6); a stress inhibiting intermediate mounting substrate 202 (col.6: 3-5) connected to carrier 204 through a first array of solder connections 212 (col.5: 13-15); intermediate mounting substrate 202 is adapted for connection to an "interposer" 226 through a second array of solder connections 214 (col.5: 17-20); intermediate mounting substrate 202 has a second CTE different than the CTE of carrier 204 and smaller than the CTE of "interposer" 226 ($CTE_{carrier\ 204}$ = 6 PPM; $CTE_{mounting\ substrate\ 202}$ = 18 PPM; $CTE_{mounting\ substrate\ 202} < CTE_{"interposer"\ 226}$; col.5: 54-55 and 63-65; col.6: 5-10).

II. Alagaratnam et al. teaches that semiconductor 206 is a large die having "by way of example, die sizes in the range of 10 mm to 20 mm. "Thus, the improved

thermal performance provided by the [stress inhibiting mounting substrate] 202 may permit a decrease in the CTE of [carrier] 204, which permits increased I/O for the [semiconductor] 206 and a larger [semiconductor] 206." (col.6: 40-46). Although Alagaratnam et al. does not explicitly teach semiconductor sizes in the range of greater than 26 mm, his teaching of semiconductor sizes 10 mm to 20 mm is clearly *only exemplary* (i.e., "by way of example;" col.6: 41-42) and consequently admits larger size semiconductors with larger I/O capability depending on the extent of the disclosed CTE compensation in the package structure of Fig. 3 that permits such larger semiconductors (col.6: 40-46). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further adjust or select the CTE value of the stress inhibiting mounting substrate 202 in the package system of Alagaratnam et al. such that a larger size semiconductor--in particular, a large semiconductor having dimension greater than 26 mm--with corresponding larger I/O capability can be accommodated in the package system, since it has been held that, where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

As to Claim 2, modified Alagaratnam et al. further discloses "interposer" 226 is a printed circuit board (col.5: 29-33).

As to Claim 3, modified Alagaratnam et al. further discloses carrier 204 is formed of a ceramic material (col.5: 51-53).

As to Claim 4, modified Alagaratnam et al. further discloses that $CTE_{carrier\ 204}$ = 6 PPM (col.5: 51-53).

As to Claim 5, modified Alagaratnam et al. further discloses the first CTE ($CTE_{carrier\ 204}$ = 6 PPM) is larger than $CTE_{semiconductor\ 206}$ = 2-4 PPM (col.2: 6-8; col.5: 51-53).

As to Claims 6 and 7, modified Alagaratnam et al. further discloses the second CTE ($CTE_{mounting\ substrate\ 202}$ = 18 PPM) is larger than the CTE of carrier 204 ($CTE_{carrier\ 204}$ = 6 PPM) (col.5: 51-55 and 63-64).

As to Claim 8, modified Alagaratnam et al. further discloses the second CTE ($CTE_{mounting\ substrate\ 202}$ = 18 PPM) is smaller than the CTE of printed circuit board 226, ($CTE_{mounting\ substrate\ 202} < CTE_{"interposer"\ 226} = CTE_{printed\ circuit\ board\ 226}$; col.5: 54-55 and 63-65; col.6: 5-10).

As to Claim 9, modified Alagaratnam et al. further discloses the second CTE is between 14 and 18 PPM ($CTE_{mounting\ substrate\ 202}$ = 18 PPM; col.5: 54-55).

As to Claim 10, modified Alagaratnam et al. further discloses solder bumps 210 positioned on carrier 204 to facilitate connection with semiconductor 206 (Fig. 3; col.5: 7-10).

As to Claim 14 (as best understood by the Examiner in view of the 35 USC § 112, 2nd paragraph rejection above), modified Alagaratnam et al. further discloses underfill resin 230 positioned between first array of solder connections 212 (Fig. 3; col.6: 47-50).

As to Claim 16, Alagaratnam et al. further discloses that mounting substrate 202 (shown in detail as mounting substrate 402 in Fig. 4A) includes signal paths 412 between a top surface 414 and a bottom surface 416 of mounting substrate 402 (col.9: 40-42).

As to Claims 17 and 21:

I. Alagaratnam et al. discloses, in Figs. 2 and 3: a chip carrier 204 having a semiconductor 206 mounted thereon, the chip carrier 204 having a first CTE between 3 and 7PPM (i.e., $CTE_{carrier\ 204}$ = 6 PPM; col.5: 51-53); a stress inhibiting mounting substrate 202 (col.6: 3-5) connected to carrier 204 through a first array of solder connections 212 (col.5: 13-15).

II. Alagaratnam et al. teaches that semiconductor 206 is a large die having "by way of example, die sizes in the range of 10 mm to 20 mm. "Thus, the improved thermal performance provided by the [stress inhibiting mounting substrate] 202 may permit a decrease in the CTE of [carrier] 204, which permits increased I/O for the [semiconductor] 206 and a larger [semiconductor] 206." (col.6: 40-46). Although Alagaratnam et al. does not explicitly teach semiconductor sizes in the range of greater than 26 mm, his teaching of semiconductor sizes 10 mm to 20 mm is clearly *only exemplary* (i.e., "by way of example;" col.6: 41-42) and consequently admits larger size semiconductors with larger I/O capability depending on the extent of the disclosed CTE compensation in the package structure of Fig. 3 that permits such larger semiconductors (col.6: 40-46). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further adjust or select the

CTE value of the stress inhibiting mounting substrate 202 in the package system of Alagaratnam et al. such that a larger size semiconductor--in particular, a large semiconductor having dimension greater than 26 mm--with corresponding larger I/O capability can be accommodated in the package system, since it has been held that, where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

As to Claim 18, Alagaratnam et al. further discloses that mounting substrate 202 has a CTE between 14 and 18 PPM ($CTE_{\text{mounting substrate 202}}$ = 18 PPM; col.5: 54-55).

As to Claim 19:

I. Alagaratnam et al. further discloses a PCB mounting substrate 226 connected to mounting substrate 202 through a second array of solder connections 214 (Fig. 3).

II. Alagaratnam et al. does not explicitly teach that the PCB mounting substrate 226 has a CTE between 14 and 17 PPM but does teach that the PCB mounting substrate 226 has a CTE of **about** 18 PPM (col.7: 33-34). Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to set the CTE of substrate 226 in the range of 14-17 PPM (i.e., **about** 18 PPM) since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

As to Claim 20:

I. Alagaratnam et al. further discloses a PCB mounting substrate 226 connected to chip carrier 204 through a second array of solder connections 214 (Fig. 3).

II. Alagaratnam et al. does not explicitly teach that the PCB mounting substrate 226 has a CTE between 14 and 17 PPM but does teach that the PCB mounting substrate 226 has a CTE of **about** 18 PPM (col.7: 33-34). Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to set the CTE of substrate 226 in the range of 14-17 PPM (i.e., **about** 18 PPM) since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

18. Claims 11 and 12 (as best understood by the Examiner in view of the 35 USC § 112, 2nd paragraph rejections, above) are rejected under 35 U.S.C. 103(a) as being unpatentable over Alagaratnam et al. in view of Jackson et al.

As to Claims 11 and 12:

I. Modified Alagaratnam et al. discloses all the limitations of base and intervening Claims 1 and 10 and further discloses that bumps 212 (between carrier 204 and mounting substrate 202) and bumps 214 (between intermediate mounting substrate 202 and PCB 226) are Sn/Pb solder bumps in the low to high melting point range (col.8: 47-67) but is silent as to the composition of solder bumps 212 connecting semiconductor 206 to carrier 204.

II. Jackson et al. discloses that bumps 22 (between carrier 20 and intermediate mounting substrate 30) and bumps 32 (between intermediate mounting substrate 30

and PCB 40) are high temperature Sn/Pb solder bumps using eutectic Sn/Pb solder paste for metal fusion (col.2: 63-66; col.3: 29-35), or, alternatively, Pb free solder bumps 22 and 32 (col.4: 1-5, 22-28 and 40-63) but is silent as to the composition of bumps 12 connecting semiconductor 10 to carrier 20.

III. Both Alagaratnam et al. and Jackson et al. use the low to high temperature solder bumps or Pb free bumps in order to establish a melting point hierarchy such that substrate "pop off" or delamination due to undesired metal reflow is prevented during assembly and operation (Alagaratnam et al., col.8: 40-67; Jackson et al., col.4: 6-21).

IV. Since both Alagaratnam et al. and Jackson et al. are both intermediate mounting substrates and both are solving the same assembly and operation problem of establishing the proper melting point hierarchy of the connection bumps, and since Jackson et al. teaches the equivalence of high temperature Sn/Pb solder and Pb free solder for the obtaining the melting point hierarchy, and further teaches that the electronics industry is moving towards Pb free components (col.4: 1-5), then the use of Pb free solder in the melting point hierarchy of the bump assembly for the multi-substrate package of Jackson et al. would have been readily recognized for use in the melting point hierarchy of the bump assembly for the multi-substrate package of Alagaratnam et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was replace the Sn/Pb solder bumps with Pb free bumps for **all** the bumps in the melting point hierarchy of the multi-substrate package of Alagaratnam et al., including the bumps between the semiconductor and carrier, the Pb free bumps

being compositionally adjusted so that the Pb free bumps at one completed level of the packaging do not excessively melt (causing substrate pop off) during a subsequent reflow step in the next level of the package assembly, as taught in the Pb free bump assembly of the multi-substrate package of Jackson et al.

19. Claim 15 (as best understood by the Examiner in view of the 35 USC § 112, 2nd paragraph rejections, above) is rejected under 35 U.S.C. 103(a) as being unpatentable over Alagaratnam et al. in view of Suzuki

I. Modified Alagaratnam et al. discloses all the limitations of base Claim 1 but does not teach a lid positioned over the chip carrier.

II. Suzuki discloses a lid 15 positioned over the chip carrier 11 (Fig. 3; col.4: 8-9) that protects the circuitry of carrier 11 and semiconductor chip 13 from dust and moisture.

III. Since both Alagaratnam et al. and Suzuki are both in the semiconductor packaging art, the protective cap, as used in the package of Suzuki, would have been readily recognized as beneficial in the semiconductor package of Alagaratnam et al.

IV. Therefore, it would have been obvious to one or ordinary skill in the art at the time the invention was made to position a lid over the chip carrier of Alagaratnam et al., as taught by Suzuki in order to protect the semiconductor chip 13 and the carrier circuitry from dust and moisture.

20. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moore et al. in view of Degani et al.

As to Claims 26 and 27:

I. Moore et al. discloses all the limitations of base Claim 22 and further discloses the use of soldering flux during package assembly and the subsequent cleaning and removal of soldering flux residue (col.4: 51-53 and 65-58) but does not indicate that the access passage 122 permits the cleaning and removal of the flux.

II. Degani et al. discloses the use of soldering flux during package assembly and further teaches the use of the access passage 30 for cleaning and removing the flux residue, thus facilitating the use of low-cost and efficient techniques for cleaning and removing flux (Figs. 3A,B; col.5: 36-49 and col.6: 10-21), as well as for providing underfill material (Fig. 4A) (col.5: 27-33).

III. Since both Moore et al. and Degani et al. use an access package in the substrate for providing underfill, and both Moore et al. and Degani et al. clean and remove flux residue after soldering, wherein Degani et al. further teaches using the access package to perform the flux cleaning and removal in order to facilitate low-cost and efficient flux cleaning and removal techniques, then it would have been readily recognized in the pertinent art of Moore et al., and obvious to one of ordinary skill in the art at the time the invention was made to use the access passage in Moore et al. for cleaning and removing flux residue as well as for providing underfill material, as taught by Degani et al.

21. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moore et al. in view of Lyne.

I. Moore et al. discloses all the limitations of base Claim 22 and further discloses an array of solder connections 98 (Fig. 5; col.6: 26-30 and 34-37) but does not teach at

least one additional row of solder connections adjacent to a row of solder connections of the array wherein the number of solder connections in the at least one additional row is less than the number of solder connections in each row of solder connections of the array of solder connections.

II. Lyne discloses a chip carrier 40 (Fig. 14) having a footprint 41 of solder connections 12 selectively depopulated (Fig. 9) such that the routing of traces, via diameter and the number of solder connections are optimized to enhance device reliability (col.3: 1-14) and further discloses a substrate 16 (shown in prior art Fig. 2) upon which is mounted the chip carrier 40, the substrate 16 inherently matching the corresponding footprint 41 in order to establish the connection to chip carrier 40, wherein the footprint 41 includes at least one additional row of solder contacts, i.e., three rows (see Fig. 9: 1) center row, 2) the row located two rows above the center row, and 3) the row located two rows below the center row) adjacent to a row of solder connections (i.e., any row above or below said three additional rows) wherein the number of solder connections 12 in the three additional rows (i.e. the **ten** solder connections, as shown in Fig. 9) is less than the number of solder connections in each row of solder connections of the array of connections forming footprint 41.

III. Since Moore et al. and Lyne both mount a chip carrier to a substrate, the arrangement of the solder connection array taught by Lyne to enhance device reliability would have been readily recognized in the pertinent art of Moore et al.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the footprint of chip carrier 102 and

corresponding footprint of substrate 106 in Moore et al. with the optimized footprint of Lyne in order to enhance the reliability of the device package of Moore et al., as taught by Lyne.

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Nguyen (US 5,477,933) discloses a chip carrier 13, interposer 28 and printed circuit motherboard 30 (Fig. 4). Interposer 28 is a printed circuit board (col.4: 18-23. Bumps 12 and 29 are Pb free (col.3: 62-col.4: 10; col.4: 25-29).

b) Ikeda et al. (US 5,973,930) discloses a chip carrier 4, interposer 6 and printed circuit motherboard 9 (Figs. 2A,B) wherein the difference in CTE between carrier 4 and interposer 6 is not more than 50% of the CTE of carrier 4 to minimize thermal stress on the solder connections 5 and pads 13 and 14 (col.5: 16-23).

c) Liu et al. (US 5,385,869) discloses an access passage 12 which permits the cleaning and removing of flux residue (col.3: 53-col.4: 5).

d) Lance, Jr. et al. (US 5,697,148) discloses the use of flux and the cleaning and removing of flux residue (col.3: 55-59; col.3: 65-col.4: 2). Also disclosed is an access passage 26 permitting the injection of underfill material (Figs. 4 and 5; col.3: 47-54).

e) Lin et al. (US 6,057,596) discloses a substrate 54 having bump connections 53 selectively omitted at the corner regions of the substrate, wherein the top and bottom

rows A and AJ, respectively, each have 25 bumps, which is less than the number of bumps in the remaining rows (Fig. 5).

f) Samaras et al. (US 5,991,161) disclose an interposer 12 with bottom surface 24 covered by pads 26 except for the corners of the bottom surface 24 (Figs. 2 and 3), wherein the number of pads 26 in the top and bottom rows of the LGA is less than the number of pads 26 in each of the remaining rows of the LGA (Fig. 3).

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin
Examiner
Art Unit 2827

jbv
April 14, 2003